UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,978	10/24/2001	Michael W. Morrow	42390P12943	1432

8791 7590 05/19/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/027,978
Filing Date: October 24, 2001
Appellant(s): MORROW, MICHAEL W.

Stuart A. Whittington
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 12, 2005 appealing from the Office action mailed June 3, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 14-28 and claims 1-13 and 29-33 have been canceled.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner : claims 14-28 are rejected under 35 U.S.C. 112, first paragraph, because the best mode contemplated by the inventor has not been disclosed.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,681,311	Gaskins et al.	January 20, 2004
6,658,538	Arimilli et al.	December 2, 2003
5,666.509	McCarthy	September 9, 1997
5,937,437	Roth et al.	August 10, 1999
4,766,537	Zolnowsky	August 23, 1988

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 23-24 and 26-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Gaskins et al., U.S. Patent No. 6,681,311, hereinafter Gaskins.

As per claim 23, Gaskins teaches the use of a system, comprising:

A processor (e.g. col. 4, lines 60-67, inherent that the processor unit within the microprocessor generates the virtual address element 132 to provide for the actual execution of the received data);

A discrete memory controller adapted to perform a table walk operation and coupled to the processor (e.g. figure 7, element 106);

A volatile memory device coupled to the discrete memory controller (e.g. figure 7, element 116 or col. 2, lines 12-20).

As per claim 24, Gaskins teaches the use of a MMU (i.e., TLB, figure 7, element 702), wherein the discrete memory controller is coupled to the processor via the MMU (e.g. figure 7, bus 154).

As per claim 26, Gaskins teaches the use of the discrete memory controller is adapted to provide address translation by using results of the table walk (e.g. col. 6, lines 2-10).

As per claim 27, Gaskins teaches the use of the discrete memory controller performs a table walk by combining a portion of a virtual address and a portion of a base address to generate an address of a descriptor (e.g. col. 5, lines 5-15 and col. 6, lines 2-10).

As per claim 28, Gaskins teaches the use of the volatile memory device is a DRAM (e.g. col. 2, lines 10-20).

3. Claims 14, 17 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al., U.S. Patent No. 6,658,538, hereinafter Arimilli.

As per claim 14, Arimilli teaches the use of an apparatus, comprising:

A memory controller (e.g. figure 2, element 24);

A table walk device connected to the memory controller (e.g. figure 2, element 78) and externally located from a memory management unit (MMU) (e.g. figure 2, element 48 or 50).

As per claim 17, Arimilli teaches the use of a TLB coupled to the table walk device (e.g. figure 2, element 49 or 51).

As per claim 20, Arimilli teaches the use of a processor coupled to the table walk device (e.g. figure 2, elements 52, 62-74 and 52) and a memory device coupled to the memory controller (e.g. figure 1, element 28).

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 14-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCarthy et al., U.S. Patent No. 5,666,509, hereinafter McCarthy in view of Roth et al., U.S. Patent No. 5,937,437, hereinafter Roth.

As per claim 14, McCarthy teaches the use of an apparatus, comprising:
A memory controller (e.g. figure 3, element 44);
A table walk device connected to the memory controller (e.g. figure 3, element 42).

McCarthy does not specifically show the use of a table walk device is externally located from a MMU. Roth shows the use of 2 MMUs (e.g. figure 1, elements 134 and 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine McCarthy and Roth because it would provide for parallel operation of the data and instruction caches. By having a DMMU and a IMMU in McCarthy two MMUs would be present where each table walk controller would be separate from the other MMU.

As per claim 15, McCarthy teaches the use of the table walk device combines a portion of the virtual address and a portion of a base address (e.g. figure 7).

As per claim 16, McCarthy teaches the use of the table walk device comprises a table base register to store a table base address (e.g. figure 7, element 70).

As per claim 17, McCarthy teaches the use of a TLB coupled to the table walk device (e.g. figure 3, element 40).

As per claim 18, McCarthy teaches the table walk device generates a descriptor and the TLB is adapted to receive the descriptor from the table walk device (e.g. col. 7, lines 63-67).

As per claim 20, McCarthy teaches a processor coupled to the table walk device (e.g. figure 1, element 14) and a memory device coupled to the memory controller (e.g. figure 2, element 30 or figure 1, element 22).

6. Claims 19, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCarthy et al., U.S. Patent No. 5,666,509, hereinafter McCarthy in view of Roth et al., U.S. Patent No. 5,937,437, hereinafter Roth and Zolnowsky, U.S. Patent No. 4,766,537.

As per claims 19, 21 and 22, McCarthy does not specifically show the use of the table walk device is adapted to receive memory access protection data, determine whether a process executing in the processor is permitted to access data stored in a memory device, or an abort signal to the processor if the process is not permitted to access data stored in the memory device. Zolnowsky shows the use of the table walk device is adapted to receive memory access protection data, determine whether a process executing in the processor is permitted to access data stored in a memory device, or an abort signal to the processor if the process is not permitted to access data stored in the memory device (e.g. col. 5, lines 9-12 and col. 11, line 50 to col. 12, line 20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zolnowsky with McCarthy because it would provide for protection against unauthorized access (e.g. col. 11, lines 50-55).

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaskins et al., U.S. Patent No. 6,681,311, hereinafter Gaskins in view of McCarthy et al., U.S. Patent No. 5,666,509, hereinafter McCarthy.

As per claim 25, Gaskins does not specifically show the use of the MMU is adapted to provide memory access protection by preventing a process executing in the processor from accessing predetermined data in the volatile memory device. McCarthy shows the use of the ATC is adapted to provide memory access protection by preventing a process executing in the processor from accessing predetermined data in the volatile memory device (e.g. figure 6 and col. 6, lines 17-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine McCarthy with Gaskins because it would provide for because it would provide for protection against unauthorized access at the earliest stage of address processing.

8. Claims 15, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al., U.S. Patent No. 6,658,538, hereinafter Arimilli in view of McCarthy et al., U.S. Patent No. 5,666,509, hereinafter McCarthy.

As per claim 15, Arimilli teaches the use of the table walk device for performing table walks during address translations using known methods (e.g. col. 11, lines 62-67), but does not specifically show the use of combines a portion of the virtual address and a portion of a base address. McCarthy shows the use of combines a portion of the virtual address and a portion of a base address (e.g. figure 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Arimilli and

McCarthy because it would provide for proper conversion of the address to locate the missing data from the cache.

As per claim 16, Arimilli teaches the use of the table walk device for performing table walks during address translations using known methods (e.g. col. 11, lines 62-67), but does not specifically show the use of the table walk device comprises a table base register to store a table base address. McCarthy shows the use of the table walk device comprises a table base register to store a table base address (e.g. figure 7, element 70).. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Arimilli and McCarthy because it would provide for proper conversion of the address to locate the missing data from the cache.

As per claim 18, Arimilli teaches the use of the table walk device for performing table walks during address translations using known methods (e.g. col. 11, lines 62-67), but does not specifically show the use of the table walk device generates a descriptor and the TLB is adapted to receive the descriptor from the table walk device. McCarthy shows the use of the table walk device generates a descriptor and the TLB is adapted to receive the descriptor from the table walk device (e.g. col. 7, lines 63-67).It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Arimilli and McCarthy because it would provide for storing the address translation performed by the table walk controller in the TLB to allow the entry to be used in future requests.

9. Claims 19, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al., U.S. Patent No. 6,658,538, hereinafter Arimilli in view of Zolnowsky, U.S. Patent No. 4,766,537.

As per claims 19, 21 and 22, Arimilli does not specifically show the use of the table walk device is adapted to receive memory access protection data, determine whether a process executing in the processor is permitted to access data stored in a memory device, or an abort signal to the processor if the process is not permitted to access data stored in the memory device. Zolnowsky shows the use of the table walk device is adapted to receive memory access protection data, determine whether a process executing in the processor is permitted to access data stored in a memory device, or an abort signal to the processor if the process is not permitted to access data stored in the memory device (e.g. col. 5, lines 9-12 and col. 11, line 50 to col. 12, line 20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zolnowsky with Arimilli because it would provide for protection against unauthorized access (e.g. col. 11, lines 50-55).

(10) Response to Argument

1. In the argument Appellant argued in substance that (1) The examiner has improperly overlooked how the skilled artisan would interpret Appellant's claimed discrete memory controller, when read in light of Appellant's specification as well as the cited reference of records. In fact, table walk logic 106 of Gaskin is part of a processor

data unit 700 (col. 9, lines 30-36) or in the processor itself and thus suffers from the latency problems of that Appellant's embodiments are intended to reduce.

In response to (1), the examiner respectfully disagrees. First of all, Appellant has failed to show any other functionality performed by the discrete memory controller other than the table walk functions described in claims 23, 26 and 27. Gaskin, col. 6, lines 3-10, discloses "if the TLB miss signal 154 indicates a miss of the TLB 102, the table walk logic 106 performs a page table walk to obtain the PTE" and controls the "outputs the PTE152." The table walk logic controls the page table walk and the outputs of the page table entry wherein the table walk functions are memory controlling functions. Also, because the table walk logic is discrete from the other devices in figure 1 of Gaskins, the table walk logic (e.g. figure 1, element 106 being distinct from els. 102, 116) is sufficient to read on Applicant's claimed limitations of a "discrete memory controller."

Next, the examiner properly interprets Appellant's claimed discrete memory controller, when read in light of Appellant's specification as well as the cited reference of records. In particular, Gaskin col. 3, lines 32-33, teaches "a data unit in a microprocessor" and col. 6, lines 3-6, "the data unit 100 comprises table walk logic 106. The table walk logic 106 receives the virtual address 132." Because a microprocessor is a central processing unit or processor unit on a chip, Gaskin, inherently teaches that the processor unit within the microprocessor generates the virtual address element 132 to provide for an actual execution of a received data. Also, because Gaskin fig. 7, teaches the data unit 700 includes TLB 702, data cache 116, miss logic 112, table walk logic 116, MTU 108, and BIU 114 but doesn't include an instruction decode and data

execution unit (i.e., a processor unit), the data unit is not a processor unit. Since the table walk logic (i.e. discrete memory controller) is a part of the data unit which is not the processor unit, the table walk logic (i.e. discrete memory controller) is not a part of the processor unit as applicant alleged. Thus, Gaskin teaches the "discrete memory controller" as claimed.

In further discussion, in light teaching of the Appellant's specification, page 5, lines 1-6 and fig. 1, "a memory controller 160 connected to MUX130" and "the bus controller 195 includes memory controller 160 and table walk device 170." Therefore, the Appellant's specification teaches the memory controller which is a part of the bus controller 195 and accessed through MUX130 also suffers from the latency problem of accesses through MUX 130.

More over, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., suffers from the latency problems of that Appellant's embodiments are intended to reduce) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Gaskin teaches, as claimed in the present application, a processor (e.g. col. 4, lines 60-67, inherent that the processor unit within the microprocessor generates the virtual address element 132 to provide for the actual execution of the received data); a discrete memory controller adapted to perform a table walk operation and coupled to the processor (e.g. figure 7, element 106; col. 6, lines 4-10).

2. In the argument, Appellant argued in substance that (2) Gaskins data unit 700 and/or its associated table walk logic 106 is not a discrete memory controller adapted to perform table walks as claimed in claim 23 and in fact Gaskins teaches that data unit 700 interfaces with a separate memory controller using processor bus 148 (col. 4, lines 60-66).

The examiner disagrees with the Appellant's argument (2). The transitional term "comprising," is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. See, e.g., > Genentech, Inc. v. Chiron Corp., 112 F.3d 495, 501, 42 USPQ2d1608, 1613 (Fed. Cir. 1997) ("Comprising" is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim.). Therefore, Gaskin table walk logic 106 is a discrete memory controller adapted to performed table walks (e.g., col. 6, lines 4-10) as claimed in claim 23 even though Gaskins also teaches other additional, unrecited memory controllers.

Further more, the Appellant's specification, page 4, lines 24 also teaches other, additional memory controller, "memory management unit (MNU) 150".

3. In the Argument, Appellant argued in substance that (3) Arimilli fails to teach a table walk device connected to the memory controller and externally located from a memory management unit as recited in claim 14 and the current specification pg. 4, lines 1-6 for proper interpretation of connected to.

The examiner disagrees with the Appellant's argument (3). The examiner generally has given words in the claim their ordinary and customary meaning unless explicitly specific and deliberate in the specification. According to page 4, lines1-6, "may be" is not specific and deliberate. Therefore, Arimilli teaches, as claimed in the present application, a memory controller (e.g. figure 2, element 24) and a table walk device connected to the memory controller (e.g. figure 2, element 78) and externally located from a memory management unit (MMU) (e.g. figure 2, element 48 or 50).

Also, Arimilli fig. 2, teaches a table walk device (e.g., el. 78) in directly contact with a memory controller (e.g., el. 50 or 48) and externally located from a memory management unit (MMU) (e.g., el. 48 or 50).

4. In the argument, Appellant argued in substance that (4) McCarthy fails to teach a table walk controller which is externally located from an MMU as recited in claim 14.

In response to appellant's arguments (4) against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the combination of McCarthy and Roth teaches a table walk controller which is externally located from an MMU as recited in claim 14. In particular, McCarthy teaches the use of an apparatus, comprising:

A memory controller (e.g. figure 3, element 44);

A table walk device connected to the memory controller (e.g. figure 3, element 42).

McCarthy does not specifically show the use of a table walk device is externally located from a MMU. Roth shows the use of 2 MMUs (e.g. figure 1, elements 134 and 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine McCarthy and Roth because it would provide for parallel operation of the data and instruction caches. By having a DMMU and a IMMU in McCarthy two MMUs would be present where each table walk controller would be separate from the other MMU.

5. In the argument, Appellant argued in substance that (5) there is no benefit to reconstruct the device of McCarthy when the device of Roth already performs parallel operations of data and instruction caches. There is no proper reason to combined references.

In response to appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, McCarthy does not specifically show the use of a table walk device is externally located from a MMU.

Roth shows the use of 2 MMUs (e.g. figure 1, elements 134 and 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine McCarthy and Roth because it would provide for parallel operation of the data and instruction caches. By having a DMMU and a IMMU in McCarthy two MMUs would be present where each table walk controller would be separate from the other MMU. Also, the examiner disagreed with the Appellant's argument (5) because Roth teaches performing parallel operations of data and instruction caches and DMMU and IMMU (e.g., fig.1 els. DMMU and IMMU and col. Col. 3, lines 45-60) and applying the teaching of Roth to the system of McCarthy to perform parallel operations of data and instruction caches and increase speed of memory accessing. Therefore, there is a proper reason for one of ordinary skill in the art to combined references and prima facie is established.

6. In the argument, appellant argued in substance that (6) the resultant combinations would fail to teach the limitation of a table walk controller connected to the memory controller and externally located from an MMU as recited in Appellant's claim 14.

The examiner disagreed with the Appellant's argument (6). The resultant combinations of McCarthy and Roth teaches a table walk controller a table walk controller connected to the memory controller and externally located from an MMU as recited in claim 14. In particular, McCarthy teaches the use of an apparatus, comprising:

A memory controller (e.g. figure 3, element 44);

A table walk device connected to the memory controller (e.g. figure 3, element 42).

McCarthy does not specifically show the use of a table walk device is externally located from a MMU. Roth shows the use of 2 MMUs (e.g. figure 1, elements 134 and 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine McCarthy and Roth because it would provide for parallel operation of the data and instruction caches. By having a DMMU and a IMMU in McCarthy two MMUs would be present where each table walk controller would be separate from the other MMU.

McCarthy does not specifically show the use of a table walk device is externally located from a MMU. Roth shows the use of 2 MMUs (e.g. figure 1, elements 134 and 124). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine McCarthy and Roth because it would provide for parallel operation of the data and instruction caches. By having a DMMU and a IMMU in McCarthy two MMUs would be present where each table walk controller would be separate from the other MMU.

7. In the argument, appellant argued in substance that (7) Zolnowsky fails to remedy the deficiencies of the proposed combination of McCarthy and Roth, this cited combination also fails to establish prima facie obviousness.

The examiner disagreed with the appellant argument (7). As stated in the examiner's responses to the appellant arguments (4)-(6), the combination of McCarthy

and Roth teaches all the limitations of claim 14 and the motivation is proper. Therefore, the combination of McCarthy, Roth, and Zolnowsky also establish prima facie obviousness.

8. In the argument appellant argued in substance that (8) McCarthy does not disclose providing memory access protection by preventing a process executing in the processor from accessing data in the nonvolatile memory device.

In response to appellant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., nonvolatile memory device) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). McCarthy teaches, as claimed in the present application, the ATC of MMU is adapted to provide memory access protection by preventing a process executing in the processor from accessing predetermined data in the volatile memory device (e.g. figure 6 and col. 6, lines 17-20).

According to col. 6, lines 17-20, McCarthy teaches a write protection bit that causes an error exception. When that error exception happens, it prevents the data within the address from being accessed.

9. In the argument, Appellants argued in substance that (9) there is no explanation why the skilled artisan would combine Gaskins and McCarthy and the motivation to combine based on the improper hindsight of the appellant's disclosure

In response to appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Gaskins does not specifically show the use of the MMU is adapted to provide memory access protection by preventing a process executing in the processor from accessing predetermined data in the volatile memory device. McCarthy shows the use of the ATC is adapted to provide memory access protection by preventing a process executing in the processor from accessing predetermined data in the volatile memory device (e.g. figure 6 and col. 6, lines 17-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine McCarthy with Gaskins by applying the teaching of providing memory access protection by preventing a process executing in the processor from accessing predetermined data in the volatile memory device as taught by McCarthy e.g. figure 6 and col. 6, lines 17-20 into the system of Gaskins because it would provide for protection against unauthorized access at the earliest stage of address processing.

In further discussion, in response to appellant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

10. In the argument, Appellants argued that (10) because McCarthy fail to teach a discrete memory controller adapted to perform a table walk operation, Gaskins and McCarthy, taken alone or in combination, fail to teach or suggest all the features appellant's claim 25.

In response to appellant's arguments (10) against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the combination of Gaskins and McCarthy teaches all the limitations of claim 25. In particular, Gaskins teaches the use of a system, comprising:

A discrete memory controller adapted to perform a table walk operation and coupled to the processor (e.g. figure 7, element 106).

In addition, Appellant has failed to show any other functionality performed by the discrete memory controller other than the table walk functions described in claims 23, 26 and 27. Gaskin, col. 6, lines 3-10, discloses "if the TLB miss signal 154 indicates a miss of the TLB 102, the table walk logic 106 performs a page table walk to obtain the PTE" and controls the "outputs the PTE152." Because the table walk logic controls the page table walk and the outputs of the page table entry wherein the table walk functions are memory controlling functions. Also, because the table walk logic is discrete from the other devices in figure 1 of Gaskins, the table walk logic (e.g. figure 1, element 106 being distinct from els. 102, 116) is sufficient to read on Applicant's claimed limitations of a "discrete memory controller."

Next, the examiner properly interprets Appellant's claimed discrete memory controller, when read in light of Appellant's specification as well as the cited reference of records. In particular, Gaskin col. 3, lines 32-33, teaches "a data unit in a microprocessor" and col. 6, lines 3-6, "the data unit 100 comprises table walk logic 106. The table walk logic 106 receives the virtual address 132." Because a microprocessor is a central processing unit or processor unit on a chip, Gaskin, inherently teaches that the processor unit within the microprocessor generates the virtual address element 132 to provide for an actual execution of a received data. Also, because Gaskin's fig. 7, teaches the data unit 700 includes TLB 702, data cache 116, miss logic 112, table walk logic 116, MTU 108, and BIU 114 but doesn't include an instruction decode and data execution unit (i.e., a processor unit), the data unit is not a processor unit. Since the table walk logic (i.e. discrete memory controller) is a part of the data unit which is not

the processor unit, therefore, the table walk logic (i.e. discrete memory controller) is not a part of the processor unit as applicant alleged. Thus, Gaskin teaches the "discrete memory controller" as claimed.

In further discussion, in light teaching of the Appellant's specification, page 5, lines 1-6 and fig. 1, "a memory controller 160 connected to MUX130" and "the bus controller 195 includes memory controller 160 and table walk device 170." Therefore, the Appellant's specification teaches the memory controller which is a part of the bus controller 195 and accessed through MUX130 also suffers from the latency problem of accesses through MUX 130.

In short, because the combination Gaskin and McCarthy teach a discrete memory controller adapted to perform a table walk operation, Gaskins and McCarthy, taken alone or in combination, teach or suggest all the features appellant's claim 25.

11. In the argument, Appellant argued that (11) Arimilli and McCarthy, taken alone or in combination, fail to teach or suggest a table walk device connected to the memory controller and externally located from a memory management unit as recited in claims 15-16 and 18.

In response to appellant's arguments (11) against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir.

1986). In this case, the combination of Arimili and McCarthy teaches a table walk device connected to the memory controller and externally located from a memory management unit as recited in claims 15-16 and 18.

In particular, the examiner generally has given words in the claim their ordinary and customary meaning unless explicitly specific and deliberate in the specification. According to page 4, lines1-6, "may be" is not specific and deliberate. Therefore, Arimilli teaches, as claimed in the present application, a memory controller (e.g. figure 2, element 24) and a table walk device connected to the memory controller (e.g. figure 2, element 78) and externally located from a memory management unit (MMU) (e.g. figure 2, element 48 or 50).

Also, Arimilli fig. 2, teaches a table walk device (e.g., el. 78) in directly contact with a memory controller (e.g., el. 50 or 48) and externally located from a memory management unit (MMU) (e.g., el. 48 or 50).

12. In the argument, Appellant argued that (12) Arimilli and Zolnowsky, taken alone or in combination, fail to teach or suggest a table walk device connected to the memory controller and externally located from a memory management unit.

In response to appellant's arguments (12) against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the combination of Arimili and Zolnowsky teaches a table walk

device connected to the memory controller and externally located from a memory management unit.

In particular, the examiner generally has given words in the claim their ordinary and customary meaning unless explicitly specific and deliberate in the specification. According to page 4, lines1-6, "may be" is not specific and deliberate. Therefore, Arimilli, as claimed in the present application, a memory controller (e.g. figure 2, element 24) and a table walk device connected to the memory controller (e.g. figure 2, element 78) and externally located from a memory management unit (MMU) (e.g. figure 2, element 48 or 50).

Also, Arimilli fig. 2, teaches a table walk device (e.g., el. 78) in directly contact with a memory controller (e.g., el. 50 or 48) and externally located from a memory management unit (MMU) (e.g., el. 48 or 50).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Denise Tran

P.P.E. 2185

Denise Tran

Conferees:

Matthew Kim

S.P.E. 2186

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Eddie Chan

S.P.E. 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100